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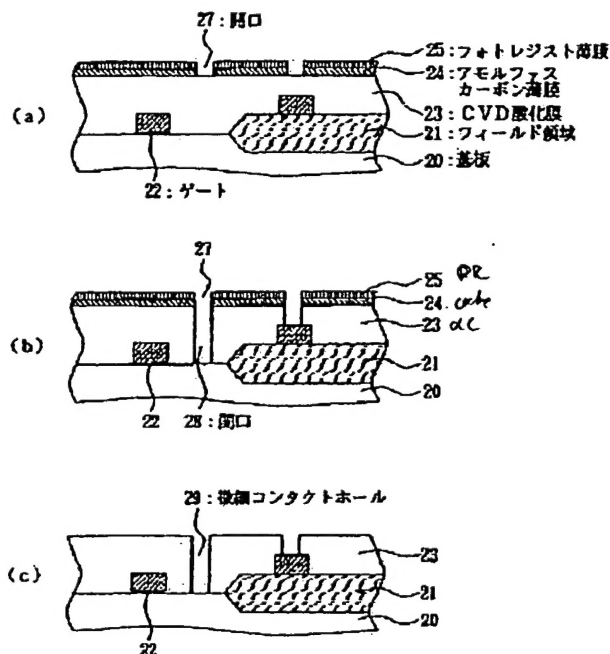
PUBLICATION NUMBER : 09045633  
 PUBLICATION DATE : 14-02-97  
 APPLICATION DATE : 26-07-95  
 APPLICATION NUMBER : 07190034

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INT.CL. : H01L 21/28 H01L 21/3065 H01L 21/768  
 H01L 21/8234 H01L 27/06

TITLE : METHOD FOR FORMING FINE HOLE  
 OF SEMICONDUCTOR INTEGRATED  
 CIRCUIT DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To easily and accurately form a fine hole with a high aspect ratio.

SOLUTION: A method for forming the fine hole of a semiconductor integrated circuit device consists of a process for forming amorphous carbon thin film 24 on CVD oxide film 23 as a lower-layer insulation film, a process for forming a photoresist thin film 25 on the amorphous carbon thin film 24, and a process for opening a contact hole 29 by performing the patterning of photolithography, etching the amorphous carbon thin film 24 with the photoresist thin film 25 as a mask, and etching the CVD oxide film 23 with the patterned amorphous carbon thin film 24 and the photoresist thin film 25 as a mask.

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CLAIMS

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[Claim(s)]

[Claim 1] (a) The process which forms an amorphous carbon thin film on a lower layer insulator layer, (b) The process which forms a photoresist thin film on this amorphous carbon thin film, (c) Perform patterning of FOTORISO and said amorphous carbon thin film is etched into a mask for said photoresist thin film. The formation approach of the detailed hole of the semiconductor integrated circuit equipment characterized by giving the process which etches said lower layer insulator layer and carries out opening of the hole by using as a mask the amorphous carbon thin film and photoresist thin film by which patterning was carried out.

[Claim 2] The formation approach of the detailed hole of the semiconductor integrated circuit equipment characterized by processing etching of said amorphous carbon thin film, and etching of said lower layer insulator layer continuously with the same equipment in the formation approach of the detailed hole of semiconductor integrated circuit equipment according to claim 1.

[Claim 3] The formation approach of the detailed hole of the semiconductor integrated circuit equipment characterized by carrying out etching processing of etching of said amorphous carbon thin film, and the etching of said lower layer insulator layer on the same chamber and the same conditions in the formation approach of the detailed hole of semiconductor integrated circuit equipment according to claim 1.

[Claim 4] The formation approach of the detailed hole of the semiconductor integrated circuit equipment characterized by carrying out etching processing on processing conditions by which said amorphous carbon thin film is etched into the outside of a photoresist mask in the shape of a forward tapered shape processing etching of said amorphous carbon thin film, and etching of said lower layer insulator layer on the same chamber and the same conditions in the formation approach of the detailed hole of semiconductor integrated circuit equipment according to claim 1.

[Claim 5] (a) The process which forms an amorphous carbon thin film on a lower layer insulator layer, (b) The process which forms a photoresist thin film on this amorphous carbon thin film, (c) The process which performs patterning of FOTORISO and etches said amorphous carbon thin film by using said photoresist thin film as a mask, (d) The formation approach of the detailed hole of the semiconductor integrated circuit equipment characterized by giving the process which etches said photoresist thin film, etches said lower layer insulator layer and carries out opening of the hole by using as a mask only the amorphous carbon thin film by which patterning was carried out.

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## DETAILED DESCRIPTION

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### [Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the formation approach of the detailed hole in semiconductor integrated circuit equipment, and relates to the formation approach of a detailed contact hole especially.

[0002]

[Description of the Prior Art] Conventionally, there was a thing as shown below as a technique of such a field. Drawing 3 is the formation process sectional view of the contact hole in conventional semiconductor integrated circuit equipment.

(a) Make 3000A – 8000A (BPSG-boron FOSUFO silicate glass etc.) of CVD oxide films 13 as an insulator layer generate first, on an active field, the field field (field field oxide film) 11, and the semiconductor substrate 10 with which the pattern of gate 12 grade is formed, as shown in drawing 3 (a).

[0003] (b) Next, as shown in drawing 3 (b), go into a FOTORISO process and apply 9000A – 12000A of photoresists 14.

(c) Subsequently, as shown in drawing 3 (c), with an exposure machine (stepper), required exposure is performed, carry out the development of this using a photo mask, remove the unnecessary part of a photoresist 14, and form opening 15.

[0004] (d) Next, carry out etching removal of the CVD oxide film 13 by using as a mask the resist pattern formed in FOTORISO after going into an etching process, carrying out etching processing using the gas plasma with a dry etching system and forming hole 16A, as shown in drawing 3 (d).

(e) Furthermore, as shown in drawing 3 (e), form contact hole 16B for the resist mask which became unnecessary ashing and by carrying out washing (for example, washing at 100 degrees C – 120 degrees C by mixed liquor of sulfuric-acid + hydrogen peroxide) removal.

[0005]

[Problem(s) to be Solved by the Invention] However, the pattern aspect ratio (ratio of the height to pattern width of face) of a contact hole is increasing quickly by improvement in the degree of integration of a semiconductor integrated circuit in recent years. It is supposed that the inclination is especially remarkable by the pattern property in a contact hole, and an aspect ratio will become even 7–10 in 4–5, and 256MbDRAM classes in 64MbDRAM classes (although explanation of the above-mentioned conventional technique has described only gate top CVD thickness, a CVD oxide film is generated by many layers in an actual process, and it becomes the thickness which also amounts to about 2 micrometers in a thick field). Since a part for resist thickness is added to this at the time of etching processing, in a 6 – 8,256MbDRAM class, it becomes 12–15 in 64MbDRAM classes.

[0006] Thus, if the aspect ratio of the pattern of a contact hole becomes high, etching processing will become very difficult and the probability for the fault of processing to occur will become high. This is said because the ion and radical required for etching in the gas plasma stop being able to reach the bottom of a hole easily. Although the device of high-vacuum-izing of etching processing etc. is made in order to solve this problem, it cannot be said that the still good solution means is found out.

[0007] This invention removes the above-mentioned trouble and aims at offering the formation

approach of the detailed hole in the semiconductor integrated circuit equipment which can form the detailed hole of a high aspect ratio easily and exactly.

[0008]

[Means for Solving the Problem] This invention is set to the formation approach of the detailed hole of (1) semiconductor-integrated-circuit equipment, in order to attain the above-mentioned purpose. The process which forms an amorphous carbon thin film on a lower layer insulator layer, and the process which forms a photoresist thin film on this amorphous carbon thin film, Perform patterning of FOTORISO and said amorphous carbon thin film is etched into a mask for said photoresist thin film. It is made to give the process which etches said lower layer insulator layer and carries out opening of the hole by using as a mask the amorphous carbon thin film and photoresist thin film by which patterning was carried out.

[0009] (2) Process etching of said amorphous carbon thin film, and etching of said lower layer insulator layer continuously with the same equipment in the formation approach of the detailed hole of the semiconductor integrated circuit equipment the above-mentioned (1) publication.

(3) Be made to carry out etching processing of etching of said amorphous carbon thin film, and the etching of said lower layer insulator layer on the same chamber and the same conditions in the formation approach of the detailed contact hole of the semiconductor integrated circuit equipment the above-mentioned (1) publication.

[0010] (4) Be made to carry out etching processing on processing conditions by which said amorphous carbon thin film is etched in the shape of a forward tapered shape on the outside of a photoresist mask although etching of said amorphous carbon thin film and etching of said lower layer insulator layer are processed on the same chamber and the same conditions in the formation approach of the detailed contact hole of the semiconductor integrated circuit equipment the above-mentioned (1) publication.

[0011] (5) The process which forms an amorphous carbon thin film on a lower layer insulator layer in the formation approach of the detailed hole of semiconductor integrated circuit equipment, The process which forms a photoresist thin film on this amorphous carbon thin film, The process which performs patterning of FOTORISO and etches said amorphous carbon thin film by using said photoresist thin film as a mask, It is made to give the process which carries out washing removal of said photoresist thin film, etches said lower layer insulator layer and carries out opening of the hole by using as a mask only the amorphous carbon thin film by which patterning was carried out.

[0012]

[Function]

[1] According to the formation approach of the detailed hole in semiconductor integrated circuit equipment according to claim 1, the amorphous carbon thin film (24) was formed on the lower layer insulator layer (CVD oxide film) (23), and the photoresist thin film (25) sharply thin-film-ized as compared with the former was formed on it.

[0013] Although a certain amount of thickness was conventionally required for the photoresist as a mask for etching a CVD oxide film, in this invention, a photoresist thin film (25) mask can attain thin film-ization that there should just be thickness which can be equal to etching of an amorphous carbon thin film (24). It has the etching-proof nature of an amorphous carbon thin film (24) several times as large as a resist, and since the amorphous carbon thin film (24) has the big effectiveness as an etching mask at the time of etching of a CVD oxide film (23), the thickness of a resist is thin and ends.

[0014] Thus, an etching aspect ratio will fall, etching of a CVD oxide film becomes easy, and expansion of an etching margin can be aimed at by having enabled thin film-ization of a resist. Furthermore, by thin-film-izing a resist, it becomes possible to improve the resolving power of a photograph pattern, and the FOTORISO margin for detailed pattern formation can be expanded.

[0015] Moreover, since an amorphous carbon thin film has the low surface reflection factor, a FOTORISO margin is expandable with this.

[2] According to the formation approach of the detailed hole in semiconductor integrated circuit equipment given in the 2nd term of a claim, compaction of the processing time which is performing consecutive processing with the same equipment and starts a transfer in etching of an amorphous carbon thin film (24) and a lower layer insulator layer (CVD oxide film) (23) can be aimed at.

[0016] [3] According to the formation approach of the detailed hole in semiconductor integrated circuit equipment given in the 3rd term of a claim In order to perform processing for etching of an amorphous carbon thin film (24) and a lower layer insulator layer (CVD oxide film) (23) on the same chamber and the same conditions, The difficult activity which detects the etching terminal point of an amorphous carbon thin film (24) when an etching pattern ratio like a contact pattern is small (if etching area is small, the signal variation at the time of an etching terminal point will become small, and terminal point detection will become difficult) highly precise detection equipment -- being needed -- it becomes possible to avoid and improvement in process tolerance can be aimed at.

[0017] Moreover, by processing on the same chamber and the same conditions, the time amount (it will take time amount, before it usually carries out vacuum suction to the first after [ processing ] background pressure when changing processing conditions, and making it after that the gas conditions for the next processing) of modification of processing conditions becomes omissible, and time amount compaction much more than the time of processing can be aimed at.

[4] According to the formation approach of the detailed hole in semiconductor integrated circuit equipment given in the 4th term of a claim A photoresist thin film (34) mask is received in an amorphous carbon thin film (33). In order to etch into the outside of a mask in the shape of a forward tapered shape (33A) and to etch a lower layer insulator layer (CVD oxide film) (31) in different direction from the amorphous carbon thin film (33) mask edge, It becomes possible to make the contact hole pattern formed smaller than a resist mask dimension, and a more detailed concentrated baton hole pattern can be formed.

[0018] By this, expansion of the doubling allowances in a FOTORISO process can be performed, defects with a gate pattern, such as short-circuit, are reduced, and improvement in the yield can be aimed at.

[5] According to the formation approach of the detailed hole in semiconductor integrated circuit equipment given in the 5th term of a claim, an amorphous carbon thin film (44) can be used as a mask in the case of etching of a lower layer insulator layer (CVD oxide film) (43), an aspect ratio can decrease more sharply than before, and the process margin of etching processing can be expanded sharply. For example, it is 15000A (although the thickness formed just before the FOTORISO process it is indicated in the example that mentioned above is 3000A - 8000A) of CVD oxide films at the time of etching conventionally. As there being a process which needs to carry out etching removal also including the CVD oxide film formed at the process before it, and etching oxidation thickness becoming thicker than the oxidation thickness usually formed immediately before When forming a 0.3-micrometer hole noting that a photoresist thin film is 10000A, the aspect ratio was 8.3, but if etching processing is performed using an amorphous carbon thin film as 1000A according to this invention, an aspect ratio can be reduced even to 5.3.

[0019] It is possible to reduce the thickness of a photoresist thin film also in this case, and to carry out photograph patterning like the case of a publication of the above (1), therefore a FOTORISO margin can be expanded.

[0020]

[Example] Hereafter, it explains to a detail, referring to a drawing about the example of this invention. The formation process sectional view (the 1) of a detailed contact hole in which drawing 1 shows the 1st example of this invention, and drawing 2 are the formation process sectional views (the 2) of the detailed contact hole.

(a) First, as shown in drawing 1 (a), generate 3000A - 8000A of CVD oxide films 23 on the substrate 20 with which an active field, the field field (field oxide) 21, and the gate 22 were formed.

[0021] (b) Next, as shown in drawing 1 (b), form 100A - 800A of amorphous carbon thin films 24 on



the CVD oxide film 23. This amorphous carbon thin film 24 may use whichever of a spatter or a CVD method.

(c) Next, as shown in drawing 1 (c), go into a FOTORISO process and apply the photoresist thin film 25 for patterning on the amorphous carbon thin film 24 by 3000Å – 6000Å thickness. It is important to make thickness of the photoresist thin film 25 as thin as possible here.

[0022] (d) Next, as shown in drawing 1 (d), perform and carry out the development of the required exposure using a photo mask with an exposure machine (stepper), remove the unnecessary part of the photoresist thin film 25, and form opening 26.

(e) Next, as shown in drawing 2 (a), carry out etching processing of the amorphous carbon thin film 24 with a plasma dry etching system by using said photoresist pattern as a mask, remove an unnecessary part, and form opening 27.

[0023] (f) Next, as shown in drawing 2 (b), carry out etching processing of the etching of the CVD oxide film 23 using a plasma dry etching system too, remove an unnecessary part, and form opening 28.

(g) Next, as shown in drawing 2 (c), the detailed contact hole 29 is formed by carrying out ashing and washing removal of the photoresist thin film (mask) which became unnecessary, and the amorphous carbon thin film 24. The amorphous carbon thin film 24 can be removed to a resist and coincidence by the conventional ashing and washing.

[0024] Thus, since it constituted, according to the 1st example, the amorphous carbon thin film 24 was formed on the CVD oxide film 23, and photoresist thickness was sharply thin-film-ized as compared with the former. Although a certain amount of thickness was conventionally required for this as a mask for a photoresist to etch a CVD oxide film, in this invention, a resist mask should just have the thickness which can be equal to etching of the amorphous carbon thin film 24. It has the etching-proof nature of the amorphous carbon thin film 24 several times as large as a resist, and since there is effectiveness as an etching mask that the amorphous carbon thin film 24 is big, at the time of etching of the CVD oxide film 23, the thickness of a resist may be thin.

[0025] Thus, an etching aspect ratio will fall, etching of a CVD oxide film becomes easy, and expansion of an etching margin is expected by having enabled thin film-ization of a resist. Furthermore, it becomes possible to improve the resolving power of a photograph pattern by thin-film-izing a resist, and expanding the FOTORISO margin for detailed pattern formation is expected.

[0026] Moreover, since an amorphous carbon thin film has the low surface reflection factor, expanding a FOTORISO margin also by this is expected. Next, the following processes can be changed in the 1st example of the above.

[1] Although etching of the amorphous carbon thin film 24 and etching of the CVD oxide film 23 were divided and were performed by drawing 2 (a) and drawing 2 (b) which carried out the 2nd example above, process by carrying out the continuation package of this by the same dry etching chamber. For example, it is SF<sub>6</sub> first by the ECR (electron cyclotron resonance) etching system. Using the mixed gas of gas and helium gas 1:9, by pressure 5mtorr and microwave power 300mA and bias power 50W, etching processing is carried out and it moves from the amorphous carbon thin film 24 to etching of the CVD oxide film 23 continuously (the change of a processing step is performed acting as a monitor with the etching terminal point detector adapting emission spectral analysis).

[0027] Moreover, etching of the CVD oxide film 23 is CHF<sub>3</sub>. Gas and CH two F<sub>2</sub> Etching processing is carried out using the gas which mixed gas by 4:1 by pressure 4mtorr and microwave power 400mA and bias power 250W. Thus, even if it processes etching of the amorphous carbon thin film 24 by the same etching chamber as the CVD oxide film 23, since vapor pressure is high, a resultant (a CF<sub>x</sub> kind is presumed) does not have a fear of polluting a chamber.

[0028] Thus, since it constituted and the same equipment performs etching of an amorphous carbon thin film and a CVD oxide film continuously according to the 2nd example, compaction of the processing time concerning a transfer can be aimed at.

[2] Although he was trying to change the etching conditions of the amorphous carbon thin film 24,

and the etching conditions of the CVD oxide film 23 in the 3rd example and also the above [1] in case it processed by carrying out the continuation package of etching of the amorphous carbon thin film 24, and the etching of the CVD oxide film 23 with the same dry etching system, process on the same conditions as follows in this example.

[0029] For example, it is helium gas and CHF<sub>3</sub> by the ECR etching system. Dry etching processing is carried out in different direction on condition that pressure 10mtorr and microwave power 150mA and bias power 130W using the mixed gas of 20:3 of gas. Moreover, even if it processes etching of the amorphous carbon thin film 24 and the CVD oxide film 23 by the same etching chamber, since the vapor pressure of a resultant is high, there is no fear of polluting a chamber.

[0030] Furthermore, since the amorphous carbon thin film 24 and the CVD oxide film 23 are etched on the same etching conditions, a contact pattern with a small pattern ratio (rate of surface ratio of the pattern to etch) does not have the need of detecting the etching terminal point of carbon, either. Thus, since it constituted, in order to perform etching of an amorphous carbon thin film and a CVD oxide film on the same chamber and the same conditions according to the 3rd example, The difficult activity which detects the etching terminal point of an amorphous carbon thin film when an etching pattern ratio like a contact pattern is small (if etching area is small, the signal variation at the time of an etching terminal point will become small, and terminal point detection will become difficult) highly precise detection equipment -- being needed -- it becomes possible to avoid and improvement in process tolerance can be aimed at.

[0031] Next, the 4th example of this invention is explained. Drawing 4 is an outline sectional view after formation of the detailed contact hole which shows the 4th example of this invention. In this drawing, in the CVD oxide film into which the active field of a substrate Si substrate and 31 are etched for 30, and 32, the gate and 33 show an amorphous carbon thin film, and 34 shows the photoresist thin film.

[0032] Although etching processing of an amorphous carbon thin film and the CVD oxide film was carried out in different direction on the same conditions, in the 3rd example of the above, etching processing of the CVD oxide film 31 is carried out for the amorphous carbon thin film 33 in different direction on the same conditions at the shape of a forward tapered shape. For example, it is helium gas and CHF<sub>3</sub> by the ECR etching system. The mixed gas of 20:2:1 of gas and two FCH<sub>2</sub> gas is used. On condition that pressure 10mtorr and microwave power 150mA and bias power 130W If etching processing of the amorphous carbon thin film 33 and the CVD oxide film 31 is carried out The amorphous carbon thin film 33 is etched into forward tapered shape-like 33A to a resist mask on the outside of a mask, and the CVD oxide film 31 is etched in different direction from the amorphous carbon thin film 33 mask edge.

[0033] The aforementioned example already described that it is satisfactory even if it carries out etching processing of the amorphous carbon thin film 33 and the CVD oxide film 31 on the same chamber and the same conditions. Since according to the 4th example an amorphous carbon thin film is etched into the outside of a mask in the shape of a forward tapered shape to a resist mask and a lower layer insulator layer (CVD oxide film) is etched in different direction from the amorphous carbon thin film mask edge as described above, the contact hole pattern formed becomes possible [ making it smaller than a resist mask dimension ], and can form a more detailed concentrated baton hole pattern.

[0034] By this, expansion of the doubling allowances in a FOTORISO process can be performed, defects with a gate pattern, such as short-circuit, are reduced, and improvement in the yield can be aimed at. Next, the 5th example of this invention is explained. The formation process sectional view (the 1) of a detailed contact hole in which drawing 5 shows the 5th example of this invention, and drawing 6 are the formation process sectional views (the 2) of the detailed contact hole.

[0035] (a) First, as shown in drawing 5 (a), form 3000A – 8000A of CVD oxide films 43 on an active field, the field field (field oxide) 41, and the substrate 40 with which the gate 42 grade was formed.

(b) Next, as shown in drawing 5 (b), form the amorphous carbon thin film 44 with 400A – 1000A

sputter or a CVD method.

[0036] (c) Next, as shown in drawing 5 (c), carry out 4000A – 10000A coating spreading of the photoresist thin film 45.

(d) Next, as shown in drawing 5 (d), an exposure machine (stepper) performs required patterning using a photo mask, remove an unnecessary part by the development, and form opening 46.

[0037] (e) Next, as shown in drawing 6 (a), perform etching processing of the amorphous carbon thin film 44 by using the photoresist thin film 45 as a mask, remove an unnecessary part, and form opening 47.

(f) Next, as shown in drawing 6 (b), carry out washing removal of the photoresist thin film 45 mask. Under the present circumstances, since there is a possibility that even required amorphous carbon may be removed when ashing processing is performed, ashing is performed only by washing (for example, washing at 100 degrees C – 120 degrees C by the mixed liquor of a sulfuric-acid + hydrogen peroxide), without using.

[0038] (g) Next, they are helium gas and CH two F2 for example, by the ECR etching system about the CVD oxide film 43, using as a mask the amorphous carbon thin film 44 which remained as shown in drawing 6 (c). Using the mixed gas of gas 20:3, plasma dry etching is performed on condition that pressure 10mtorr and microwave power 150mA and bias power 130W, an unnecessary part is removed, and opening 48 is formed.

[0039] (h) If ashing washing finally removes the amorphous carbon thin film 44 which became unnecessary as shown in drawing 6 (d), the detailed contact hole 49 will be formed. Depending on the case, only ashing processing is [ but ] possible for removal of this amorphous carbon thin film 44. As described above, according to the 5th example, only the amorphous carbon thin film 44 can be used as a mask in the case of etching of the CVD oxide film 43, an aspect ratio decreases more sharply than before, and the process margin of etching processing is expanded sharply. For example, it is 15000A (although it is 3000A – 8000A, the thickness formed just before the FOTORISO process it is indicated in the example that mentioned above) of CVD oxide films at the time of etching conventionally. As the process etched also including the CVD oxide film formed at the process before it being required, and etching oxidation thickness becoming thicker than the oxidation thickness usually formed immediately before When forming a 0.3-micrometer hole noting that a photoresist thin film is 10000A, the aspect ratio was 8.3, but if etching processing is performed using an amorphous carbon thin film as 1000A according to this invention, an aspect ratio can be reduced even to 5.3.

[0040] It is possible to reduce photoresist thickness also in this case and to carry out photograph patterning like the 1st example of the above, therefore expansion of a FOTORISO margin can be expected. Although the old example has described the case of the so-called contact hole formation for the metal wiring connection with an active field or the gate, this invention is applicable also to the so-called formation of the through hole for connecting metal wiring and metal wiring.

[0041] In addition, this invention is not limited to the above-mentioned example, and based on the meaning of this invention, various deformation is possible for it and it does not eliminate these from the range of this invention.

[0042]

[Effect of the Invention] As mentioned above, according to this invention, the following effectiveness can be done so as explained to the detail.

(1) According to invention given in the 1st term of a claim, the amorphous carbon thin film was formed on the lower layer insulator layer (CVD oxide film), and the photoresist thin film sharply thin-film-ized as compared with the former was formed on it. Although a certain amount of thickness was conventionally required for the photoresist as a mask for etching a CVD oxide film, in this invention, a resist mask can attain thin film-ization that there should just be thickness which can be equal to etching of an amorphous carbon thin film.

[0043] Thus, an etching aspect ratio will fall, etching of a CVD oxide film becomes easy, and



expansion of an etching margin can be aimed at by having enabled thin film-ization of a resist. Furthermore, by thin-film-izing a resist, it becomes possible to improve the resolving power of a photograph pattern, and the FOTORISO margin for detailed pattern formation can be expanded. [0044] Moreover, since an amorphous carbon thin film has the low surface reflection factor, a FOTORISO margin is expandable with this.

(2) According to invention given in the 2nd term of a claim, the same equipment is performing etching of an amorphous carbon thin film and a lower layer insulator layer (CVD oxide film) continuously, and compaction of the processing time concerning a transfer can be aimed at.

[0045] (3) In order to perform etching of an amorphous carbon thin film and a lower layer insulator layer (CVD oxide film) on the same chamber and the same conditions according to invention given in the 3rd term of a claim, The difficult activity which detects the etching terminal point of an amorphous carbon thin film when an etching pattern ratio like a contact pattern is small (if etching area is small, the signal variation at the time of an etching terminal point will become small, and terminal point detection will become difficult) highly precise detection equipment -- being needed -- it becomes possible to avoid and improvement in process tolerance can be aimed at.

[0046] Moreover, by processing on the same chamber and the same conditions, the time amount (it will take time amount, before it usually carries out vacuum suction to the first after [ processing ] background pressure when changing processing conditions, and making it after that the gas conditions for the next processing) of modification of processing conditions becomes omissible, and time amount compaction much more than the time of processing can be aimed at.

(4) Since according to invention given in the 4th term of a claim an amorphous carbon thin film is etched into the outside of a mask in the shape of a forward tapered shape to a resist mask and a lower layer insulator layer (CVD oxide film) is etched in different direction from the amorphous carbon thin film mask edge, it becomes possible to make the contact hole pattern formed smaller than a resist mask dimension, and a more detailed concentrated baton hole pattern can be formed.

[0047] By this, expansion of the doubling allowances in a FOTORISO process can be performed, defects with a gate pattern, such as short-circuit, are reduced, and improvement in the yield can be aimed at.

(5) According to invention given in the 5th term of a claim, only an amorphous carbon thin film can be used as a mask in the case of etching of a lower layer insulator layer (CVD oxide film), an aspect ratio can decrease more sharply than before, and the process margin of etching processing can be expanded sharply.

[0048] Moreover, it is possible to reduce photoresist thickness also in this case and to carry out photograph patterning like the case of a publication of the above (1), therefore a FOTORISO margin can be expanded.

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**DESCRIPTION OF DRAWINGS**

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[Brief Description of the Drawings]

[Drawing 1] It is the formation process sectional view (the 1) of a detailed contact hole showing the 1st example of this invention.

[Drawing 2] It is the formation process sectional view (the 2) of a detailed contact hole showing the 1st example of this invention.

[Drawing 3] It is the formation process sectional view of the contact hole in conventional semiconductor integrated circuit equipment.

[Drawing 4] It is an outline sectional view after formation of the detailed contact hole which shows the 4th example of this invention.

[Drawing 5] It is the formation process sectional view (the 1) of a detailed contact hole showing the 5th example of this invention.

[Drawing 6] It is the formation process sectional view (the 2) of a detailed contact hole showing the 5th example of this invention.

[Description of Notations]

20 40 Substrate

21 41 Field field (field oxide)

22, 32, 42 Gate

23, 31, 43 CVD oxide film

24, 33, 44 Amorphous carbon thin film

25, 34, 45 Photoresist thin film

26, 27, 28, 46, 47, 48 Opening

29 49 Detailed contact hole

30 Active Field of Substrate Si Substrate

33A The shape of a forward tapered shape

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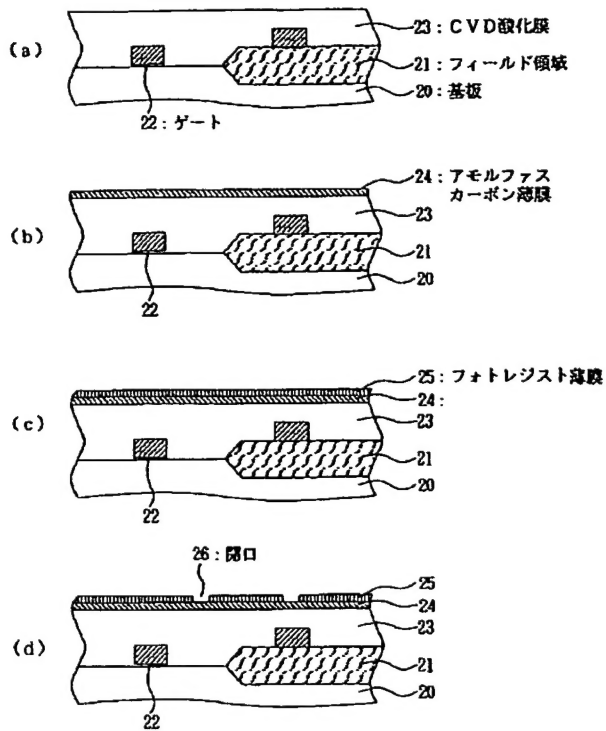
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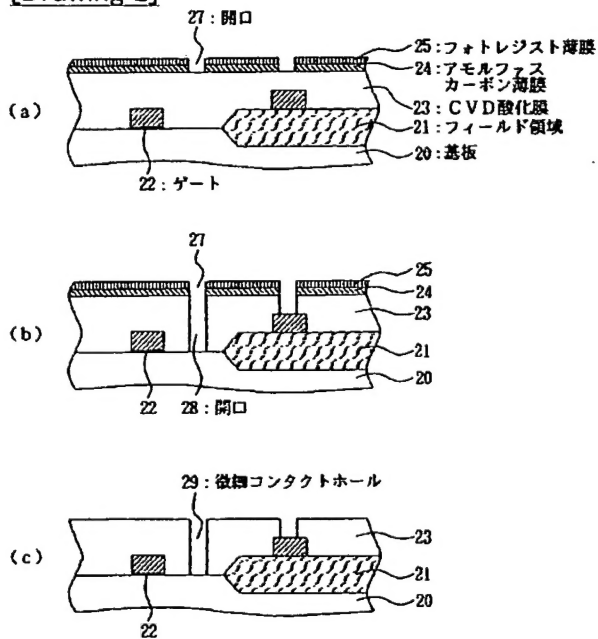
DRAWINGS

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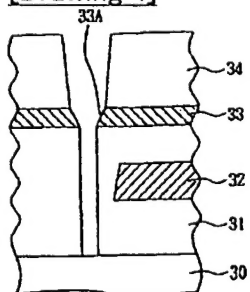
[Drawing 1]



[Drawing 2]



[Drawing 4]



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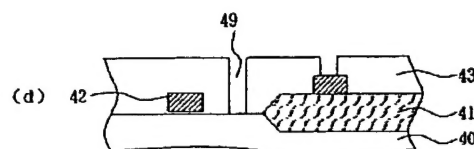
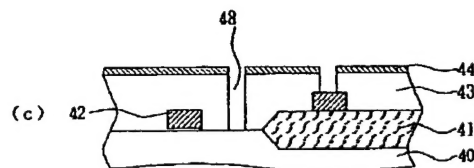
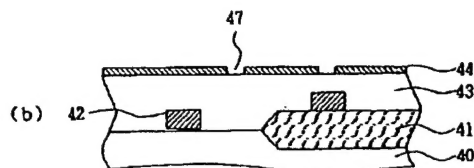
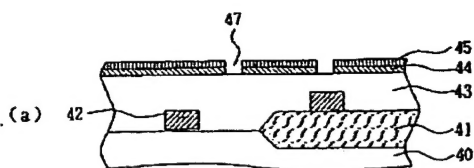
Figure 1 consists of five cross-sectional views of a semiconductor device, labeled (a) through (e). Each view shows a substrate 10 with a patterned layer 11. In view (a), a small rectangular layer 12 is on top of 11. In view (b), a larger rectangular layer 13 is added on top of 12. In view (c), three rectangular layers 14 are added on top of 13. In view (d), a layer 16A is added on top of 14. In view (e), a layer 16B is added on top of 14.

Figure 1 consists of four cross-sectional views of a semiconductor device, labeled (a) through (d). Each view shows a substrate (42) with a gate oxide layer (40) and a gate electrode (41). In (a), the gate oxide layer (40) is formed on the substrate (42) and the gate electrode (41). In (b), the gate oxide layer (40) is being etched away from the gate electrode (41). In (c), the gate oxide layer (40) is being etched away from the gate electrode (41). In (d), the gate oxide layer (40) is being etched away from the gate electrode (41). The gate electrode (41) is shown as a rectangular block on the substrate (42). The gate oxide layer (40) is shown as a hatched area. The substrate (42) is shown as a solid area. The gate oxide layer (40) is formed on the substrate (42) and the gate electrode (41). In (b), the gate oxide layer (40) is being etched away from the gate electrode (41). In (c), the gate oxide layer (40) is being etched away from the gate electrode (41). In (d), the gate oxide layer (40) is being etched away from the gate electrode (41). The gate electrode (41) is shown as a rectangular block on the substrate (42). The gate oxide layer (40) is shown as a hatched area. The substrate (42) is shown as a solid area. The gate oxide layer (40) is formed on the substrate (42) and the gate electrode (41). In (b), the gate oxide layer (40) is being etched away from the gate electrode (41). In (c), the gate oxide layer (40) is being etched away from the gate electrode (41). In (d), the gate oxide layer (40) is being etched away from the gate electrode (41).

[Drawing 6]

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[Translation done.]

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